

# Pauli-Based Computation on QLDPC Codes

A tutorial on surgery and surgery-based architectures

Sunny Zhiyang He @ Benasque, August 2026



# Outline

- I. Fault-tolerant quantum computation in 2026
- II. Code surgery via graphs and chain maps
- III. Surgery-based architectures
- IV. Further techniques in surgery
- V. Future directions

# **Fault-tolerant quantum computation in 2026**

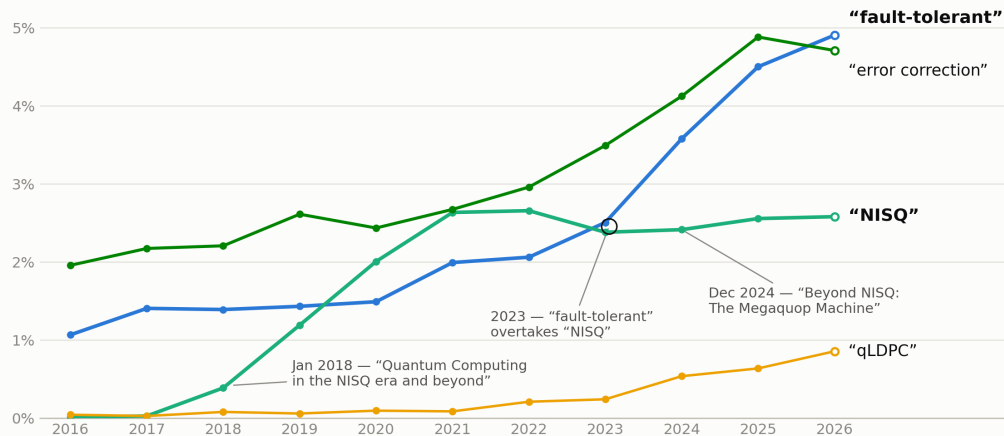
# Now is the time for FTQC

**2018:** “Because of the very hefty overhead cost of quantum error correction, **the era of fault-tolerant quantum computing (FQTC) may still be rather distant**. No one really knows how long it will take to get there.” — John Preskill, “Quantum Computing in the NISQ era and beyond”

**2026:** Industries converge to fault-tolerance, aim to deliver **hundreds to thousands of logical qubits, from megaquop to teraquop**, before 2030.

## From NISQ to FTQC

Share of new quant-ph abstracts mentioning each term, by year of submission



arXiv abstracts, cat:quant-ph, by submission year; phrases stemmed. Open markers: 2026 through Jul 14.

# Convergence of experiments and QEC theory

## QEC Theory

2019+: New theory for QLDPC codes, leading to asymptotically good codes in 2021

2019+: New decoding algorithms, focus on BP and ML

2020+: Development of simulation software, such as STIM and better decoders

2023+: Focus on finite-size QLDPC codes and their implementation on hardware

2023+: Computational methods for LDPC codes, including QLDPC surgery and transversal logic

## Experiments

2022+: Reconfigurable qubits enable non-local connectivity

2023+: Sub-threshold surface code memory, larger code gives more error suppression

2023+: Long-range connection that supports modular architectures

2024+: Magic state distillation and cultivation, gate teleportation

Consistently: Lower gate error rate, larger systems, better physical control

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Finite-scale proposals to reduce space overhead, with focus on LDPC codes

New hardware capabilities, lower physical and logical error rates, larger scale systems

# Result of fusion: new proposals of finite-size FTQC

## Gidney 2025 estimate [2505.15917]:

- Surface code architecture with lattice surgery, applied magic state cultivation and code concatenation.
- RSA-2048 in less than 1 million qubits, less than 1 week, on superconducting qubits.

## IBM Bicycle Architecture [2506.03094]:

- Modular LDPC architecture, computation by LDPC surgery.
- Roughly 10 times less qubits and 10 times slower than surface codes.

## Iceberg [2602.11457]:

- Modular LDPC architecture, computation by LDPC surgery.
- RSA-2048 in 100000 qubits, 30000 days, on neutral atoms.

## Oratomic [2603.28627]:

- Modular LDPC architecture with high-rate codes, computation by LDPC surgery.
- ECC-256 in 10000 qubits, 1000 days, on neutral atoms. RSA-2048 in 11000 qubits, 43000 days.

**More recent proposals:** IonQ Walking Cat [2604.19481], Duke + UT Austin + Yale [2604.19735], QuEra's LDPC STAR [2606.25011], Google's modular hyperbolic architecture [presented at QEC26], and more.

### Caution

These are proposals and estimates, not finalized reports. Some assumptions and methods are under discussion in the community.

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### Observation 1

All (except Gidney's) architectures are done with LDPC codes. We see **dramatic reduction in space overhead**, which has been the key bottleneck for FTQC.

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### Observation 2

LDPC surgery serves as the computational backbone for half of these proposals.

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### Observation 3

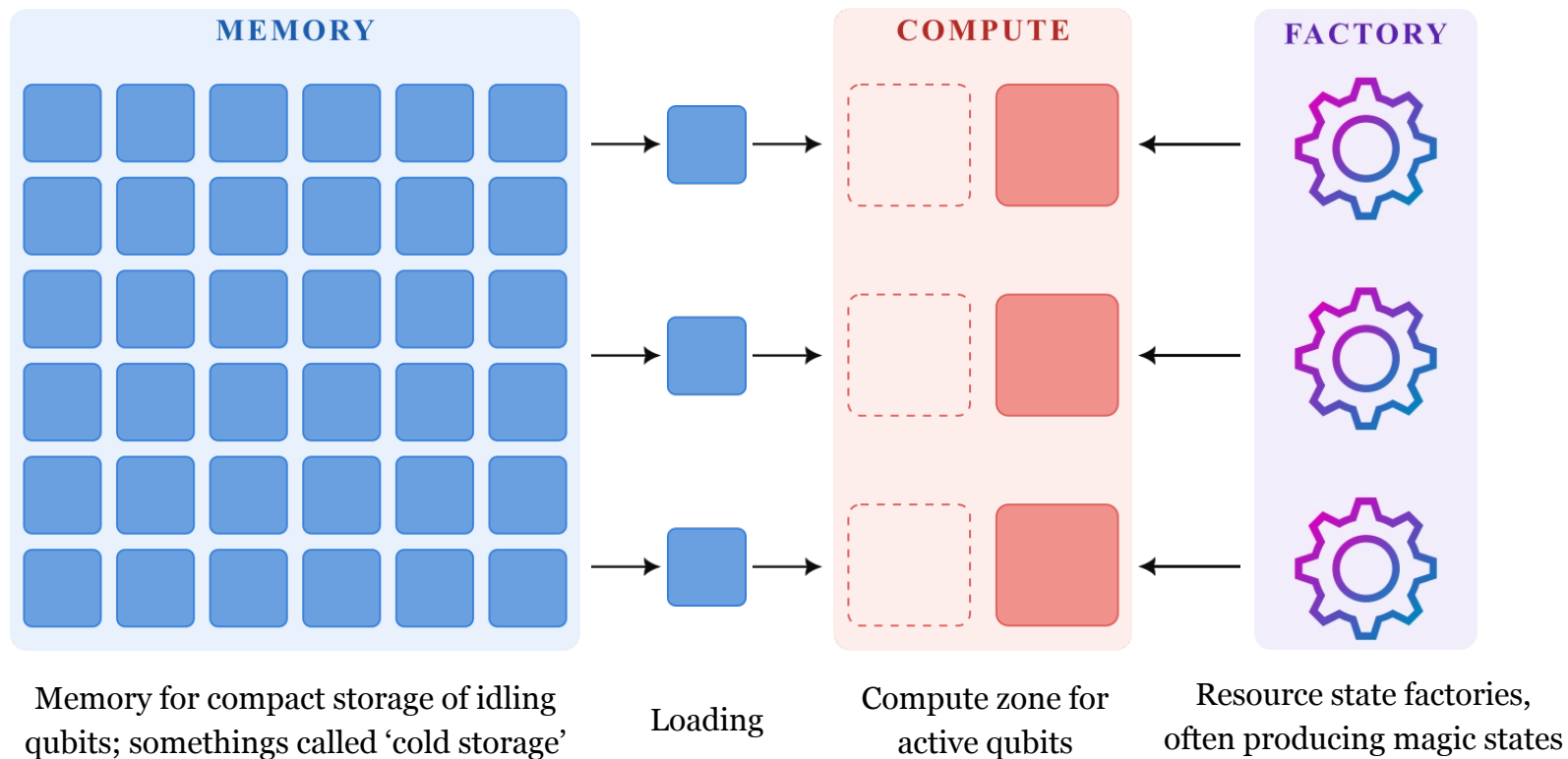
Significant increase in time cost,  
to the point of infeasible.

Is this fundamental?

❖ No, not yet.

## **Modern QLDPC architectures**

# Sketch of current architectures

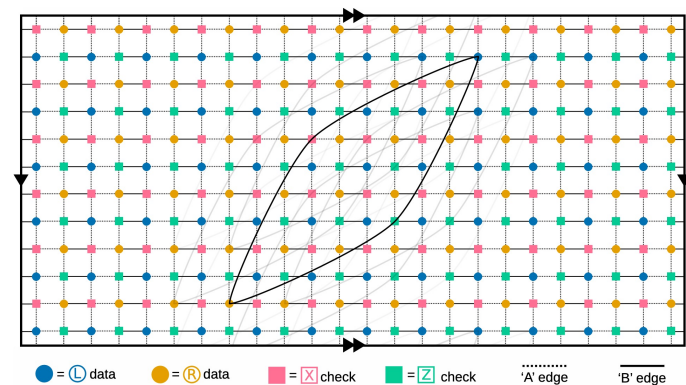


# Memory with QLDPC codes

Quantum low-density parity-check (LDPC) codes have **high encoding rate, at the cost of higher connectivity** requirement. Examples:

- Bivariate Bicycle code [144, 12, 12]<sup>[1]</sup>
- Lifted/balanced product code [544, 80, ≤ 12]<sup>[2]</sup>
- APM Codes [1152, 580, ≤ 12]<sup>[3]</sup>

Surface code: [144, 1, 12]. **Space overhead of encoding can be reduced by more than 100x!**



IBM's bivariate bicycle code

Common memory designs:

- Few big blocks
- Many small blocks
- Concatenated codes<sup>[4,5]</sup>

Tradeoff among modularity, space-efficiency, and access speed.

$$H_X = \begin{pmatrix} F_0 & F_1 & F_2 & F_3 & F_4 & F_5 & G_0 & G_1 & G_2 & G_3 & G_4 & G_5 \\ F_5 & F_0 & F_1 & F_2 & F_3 & F_4 & G_5 & G_0 & G_1 & G_2 & G_3 & G_4 \\ F_4 & F_5 & F_0 & F_1 & F_2 & F_3 & G_4 & G_5 & G_0 & G_1 & G_2 & G_3 \end{pmatrix}$$

$$H_Z = \begin{pmatrix} G_0^T & G_5^T & G_4^T & G_3^T & G_2^T & G_1^T & F_0^T & F_5^T & F_4^T & F_3^T & F_2^T & F_1^T \\ G_1^T & G_0^T & G_5^T & G_4^T & G_3^T & G_2^T & F_1^T & F_0^T & F_5^T & F_4^T & F_3^T & F_2^T \\ G_2^T & G_1^T & G_0^T & G_5^T & G_4^T & G_3^T & F_2^T & F_1^T & F_0^T & F_5^T & F_4^T & F_3^T \end{pmatrix}$$

APM codes of rate 1/2

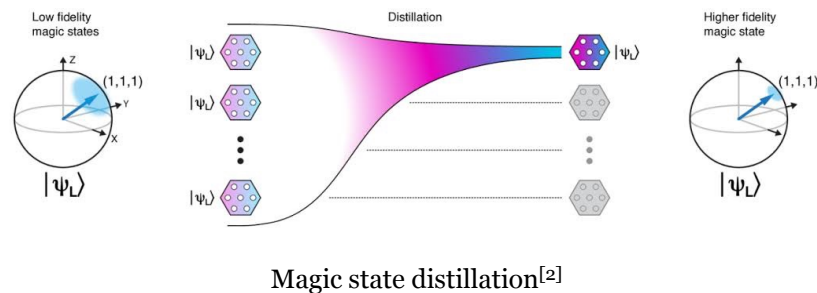
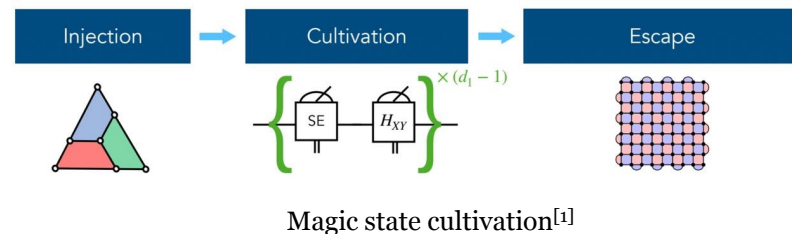
# Resource state factories

Almost all FTQC proposals use resource states, notably magic states for T and CCZ gates.

Recent architectures combine two primitives:

- **Magic state cultivation:** prepare a good ( $10^{-5\sim 9}$ ) magic state at low distance, rapidly escape into large distance surface code.
- **Magic state distillation:** take many magic states at large distance, distill them into fewer states of better quality ( $10^{-12}$  and less).
- Typical factory: **cultivate first in surface code, load into LDPC codes and distill.**

**Magic state production is one of the key bottlenecks in current QLDPC architectures!** More on that later.



# Computation machinery

For LDPC codes, we have two main methods of computation:

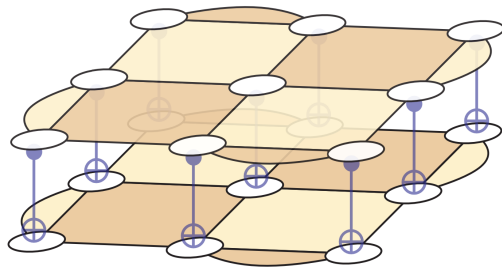
**low-depth unitaries** and **Pauli measurements**.

Low-depth unitaries:

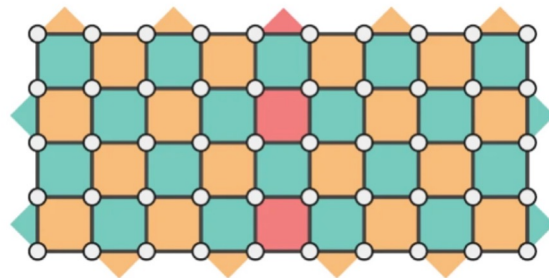
- Typical example: transversal CNOT
- Constant-depth physical circuits that implement a logical unitary
  - + **Parallel, fast, no space overhead**
  - **Logical control is constrained and often limited**
  - **Usually needs qubit reconfiguration**

Pauli measurements:

- Usually implemented by code surgery, sometimes by CAT states
- Compute by extracting Pauli observables from logical qubits.
  - + **Complete logical control, can work with fixed connectivity**
  - **Usually slower, logical control is sequential in many cases**



Transversal CNOT on surface code<sup>[1]</sup>



Lattice surgery<sup>[2]</sup>

# Why surgery now?

LDPC surgery<sup>[1-6]</sup> is a new technique that has advanced rapidly.

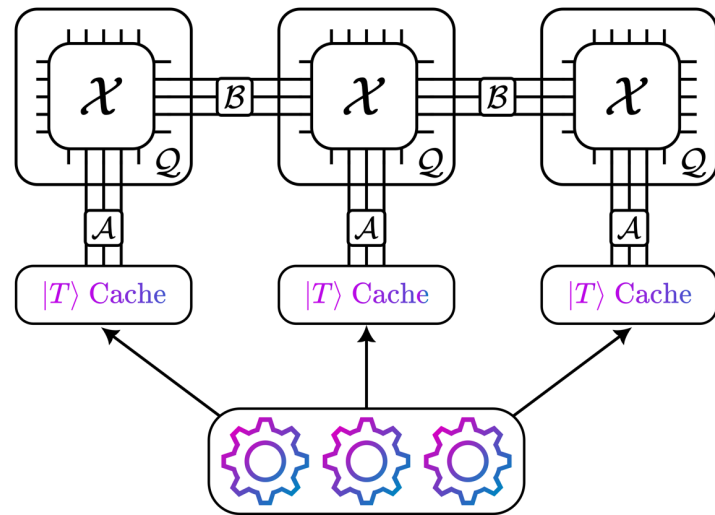
Modern surgery techniques has many desirable properties:

- Provably fault-tolerant and low-overhead<sup>[3,4]</sup>
- Complete logical control (often sequential)<sup>[6]</sup>
- Effective starting at small scale: <400 physical qubits enable control of 11 logical qubits at distance 12<sup>[2,7]</sup>
- Implementable on different qubit platforms, including fixed-connectivity hardware<sup>[4,6]</sup>

Surgery and low-depth unitaries are similar to CPU and GPU:

sequential and complex control, vs. parallel and structured control.

- In early FTQC, as we want to implement specific tasks ASAP, surgery is a very natural choice.



Extractor architecture for  
LDPC surgery-based FTQC<sup>[6]</sup>

<sup>1</sup>[Cohen et al. 2110.10794], <sup>2</sup>[Cross et al. 2407.18393], <sup>3</sup>[Williamson & Yoder 2410.02213], <sup>4</sup>[Ide et al. 2410.02753], <sup>5</sup>[Swaroop et al. 2410.03628],

<sup>6</sup>[He et al. 2503.10390]. <sup>7</sup>[IBM 2506.03094]

# If FTQC is like printing...

Suppose you have two different printing presses:

- One that prints 5 words at a time, any words of your choice;
- Another that prints 100 copies of one chosen word at a time;

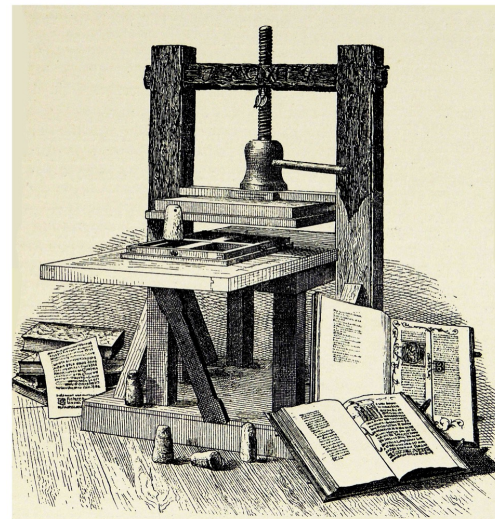
When resource is limited and you really want to print one specific essay, use the first press

- This is **sequential surgery**, which was studied in [1, 2] and adopted in recent QLDPC architectures;

When you want to print many copies of the same essay, use the second press

- This is **batched, parallel computation via transversal gates**<sup>[3]</sup>

\* Surgery can give parallel, structured logical control<sup>[4]</sup> as well, more on that later.



# **Code surgery via graphs and chain maps**

# Universal computation via logical measurements

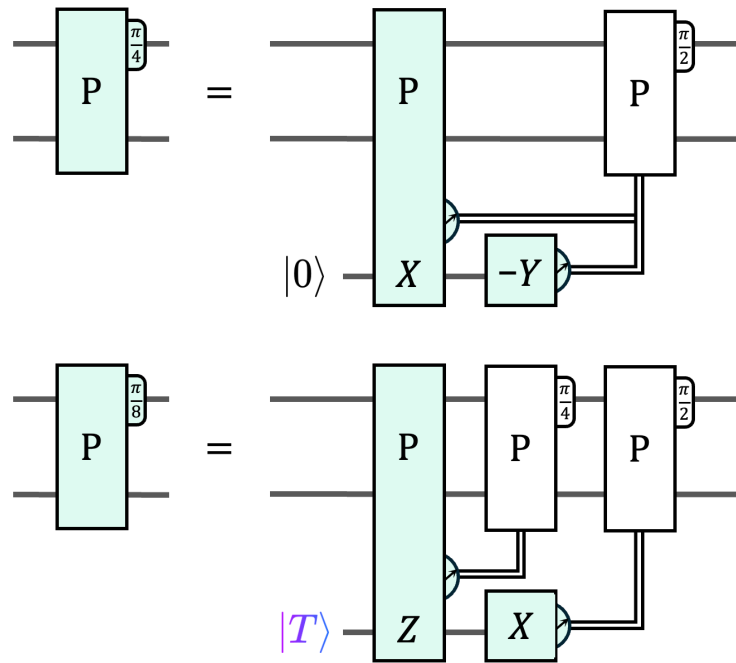
A Clifford + T circuit can be compiled into two primitives:

1. measurement of Pauli observables  
(Pauli-product measurements, PPMs)
2. magic states production

This is called **Pauli-based computation**.

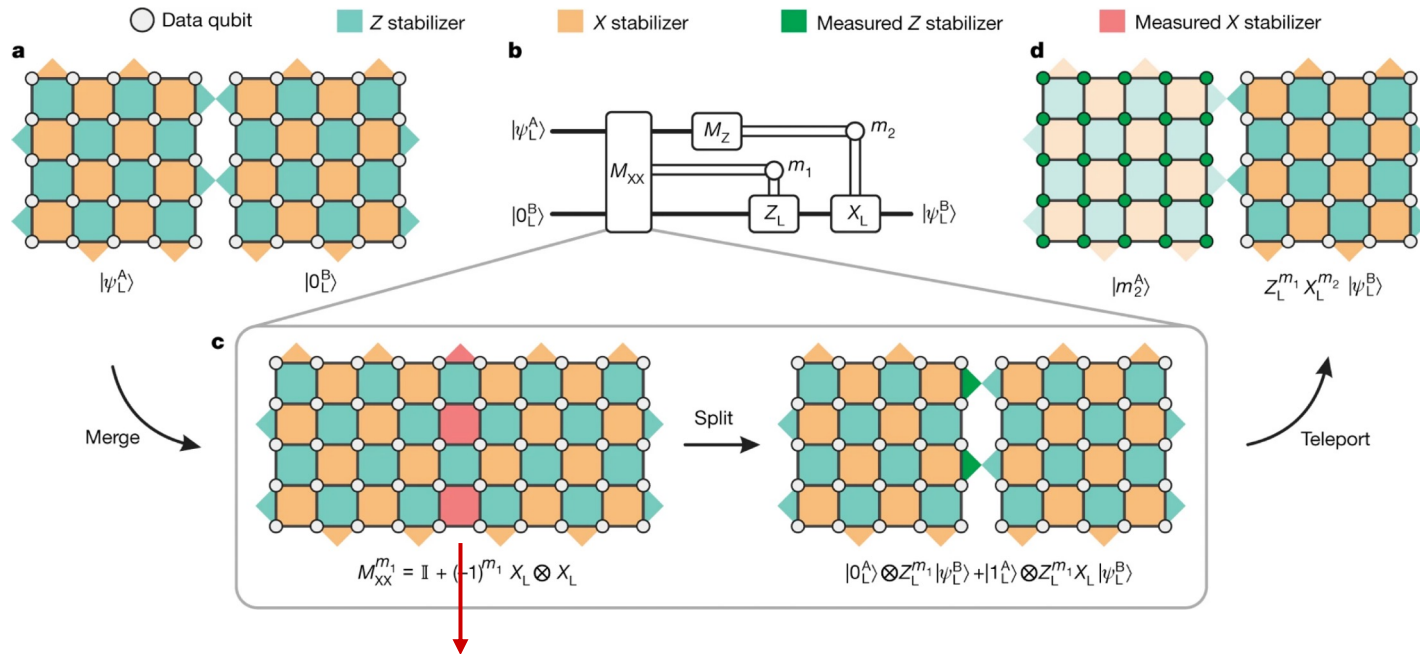
Code surgery is a way to measure logical Pauli observables fault-tolerantly.

- Starting at a quantum code (a stabilizer group), we measure a new stabilizer group, where the (large) logical Pauli become a product of (small) new stabilizers.
- Weight reduction → fault-tolerance



# Surface Code Lattice Surgery

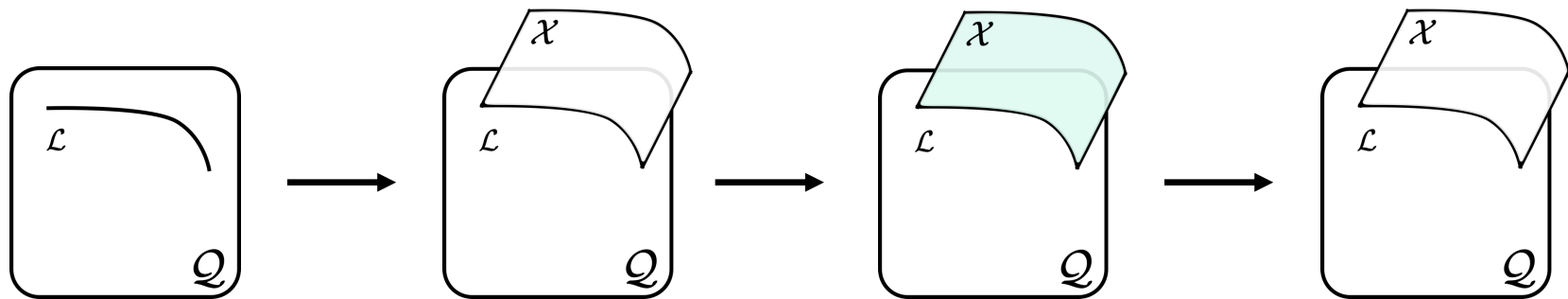
Logical measurements on surface codes: **lattice surgery**, [Horsman et al, 1111.4022].



Product of **red** X-checks =  $X_L \otimes X_L$  – **obtain logical measurement result by measuring new stabilizers.**

# Generalized Code Surgery

High level description: for a quantum code  $Q$  and a logical operator  $\mathcal{L}$ , define a new stabilizer group supported on  $Q$  and an ancilla system  $\mathcal{X}$ . Measure the new stabilizer group to measure  $\mathcal{L}$ .



(a) Start: Code  $Q$  and operator  $\mathcal{L}$ .

(b) Init: Initialize ancilla qubits in product state.

(c) Merge: Code deformation by measuring new stabilizers

(d) Split: Measure out ancilla and return to  $Q$ .

# **Code surgery via graphs and chain maps**

Graph formalism

# Scalable Tanner Graphs

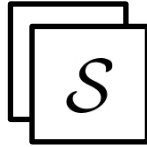
# Scalable Tanner Graphs



Code  $Q$

Physical qubits of the code  $Q$

# Scalable Tanner Graphs



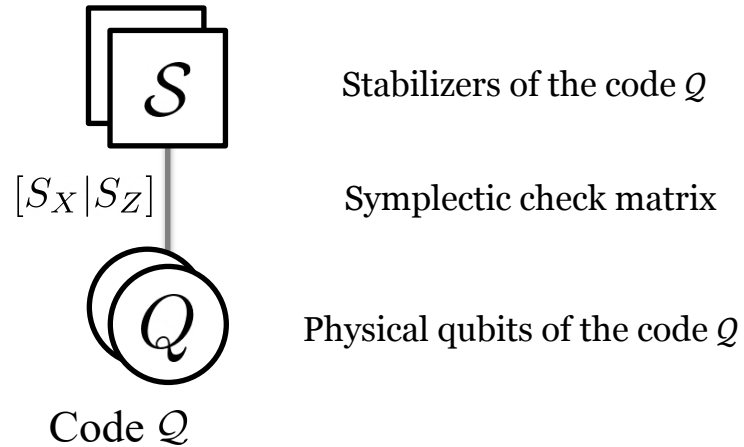
Stabilizers of the code  $\mathcal{Q}$



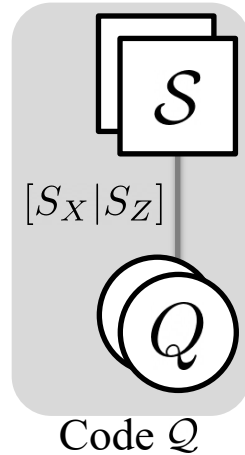
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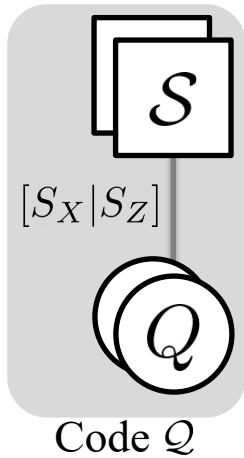


Stabilizers of the code  $Q$

Symplectic check matrix

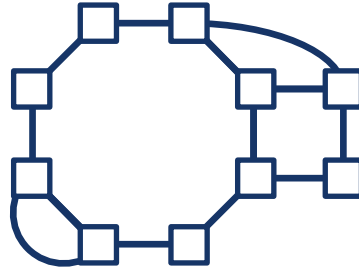
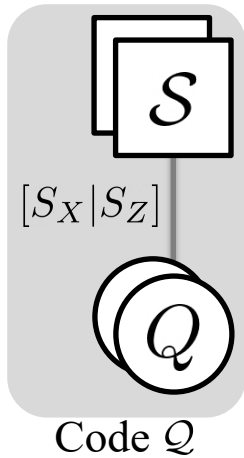
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# Building Ancilla Systems from (Hyper)Graphs



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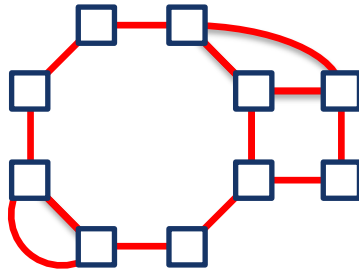
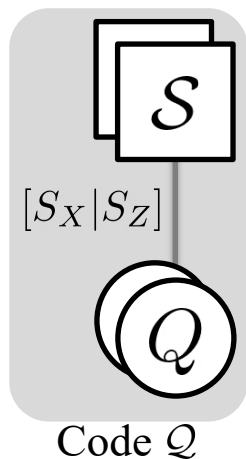
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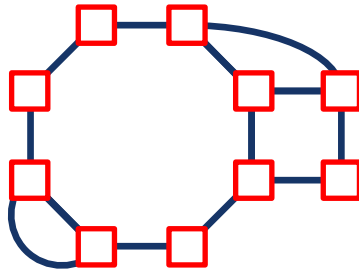
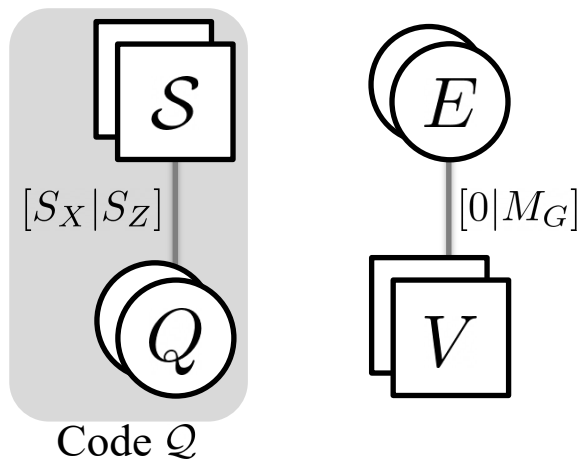
1. For every (hyper)edge in  $E$ , create an ancilla edge qubit.



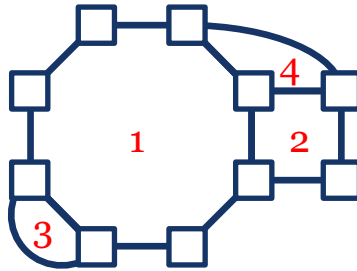
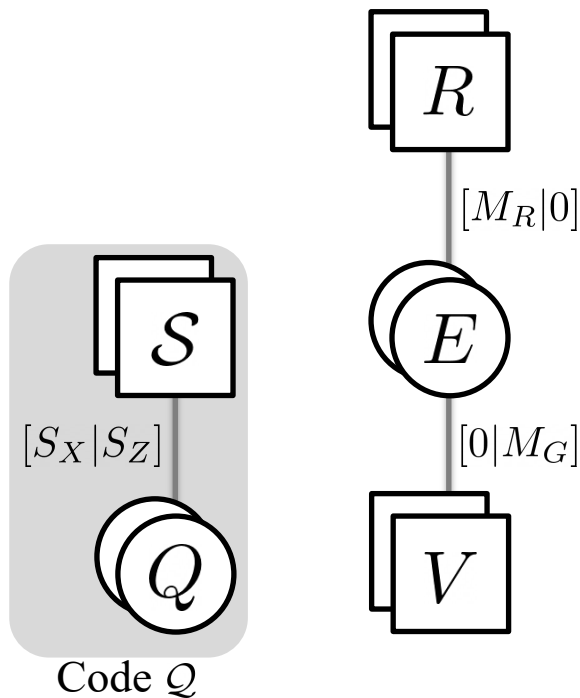
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Let  $G = (V, E)$  be a (hyper)graph.

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2. For every vertex in  $V$ , create an **vertex check**, which act on adjacent edge qubits by Pauli  $Z$ .



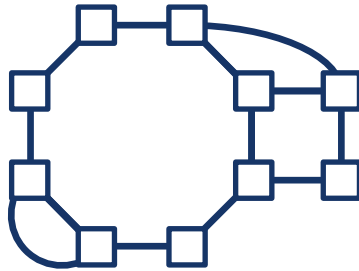
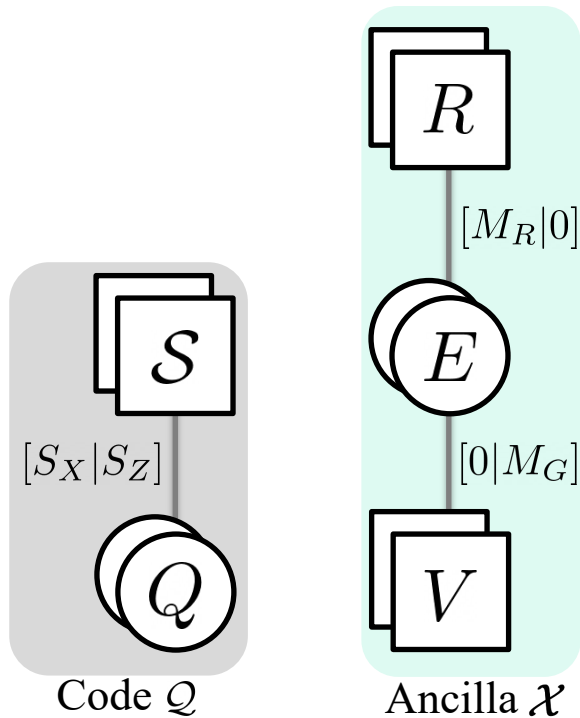
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3. Pick a **cycle basis  $R$**  of  $G$ . **For every cycle  $C$  in  $R$ , create a cycle check**, which act on edges in  $C$  by Pauli  $X$ .

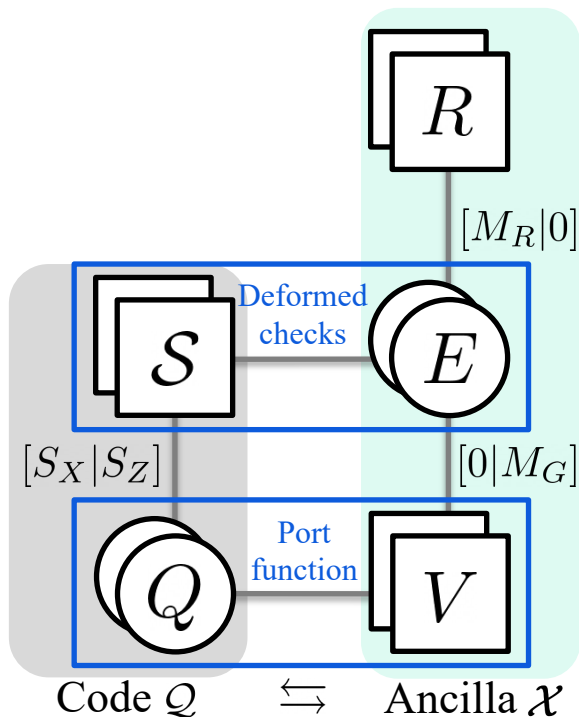
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# Extracting Logical Pauli Observables



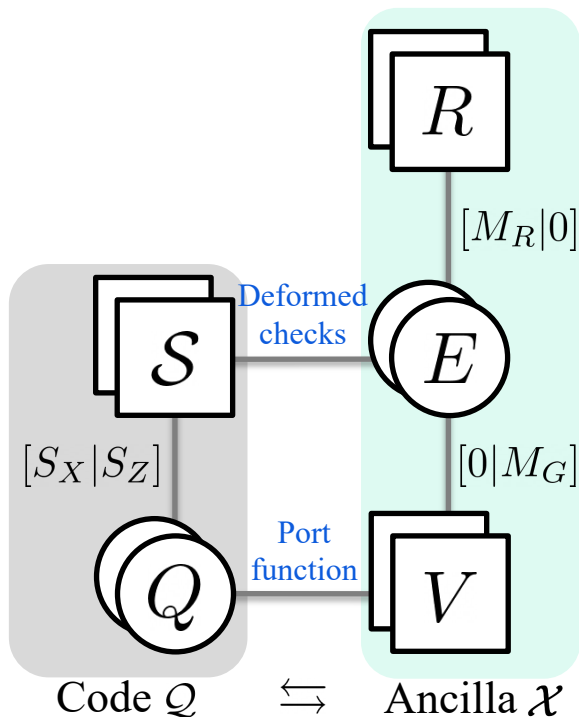
To measure a logical operator  $\mathcal{L}$ , we construct:

1. **Measurement (hyper)graph  $G$** ;
2. **Port function**: Pauli actions of vertex checks  $V$  on qubits of  $Q$ ; Defined so that **product of vertex checks in a connected component equals  $\mathcal{L}$** .
3. **Deformed checks**: Pauli actions of stabilizers  $S$  on ancilla edge qubits  $E$ .

These data defines a subsystem code, which we call the **measurement code**  $Q_{\mathcal{L}}$ .

This formalism is developed gradually in [1-5]. See Section 3 of [5] for a short technical review.

# Parallel Surgery via Hypergraphs



Measurements = **kernel of adjacency matrix of G**  
= sets of vertices that have even overlap with every hyperedge.

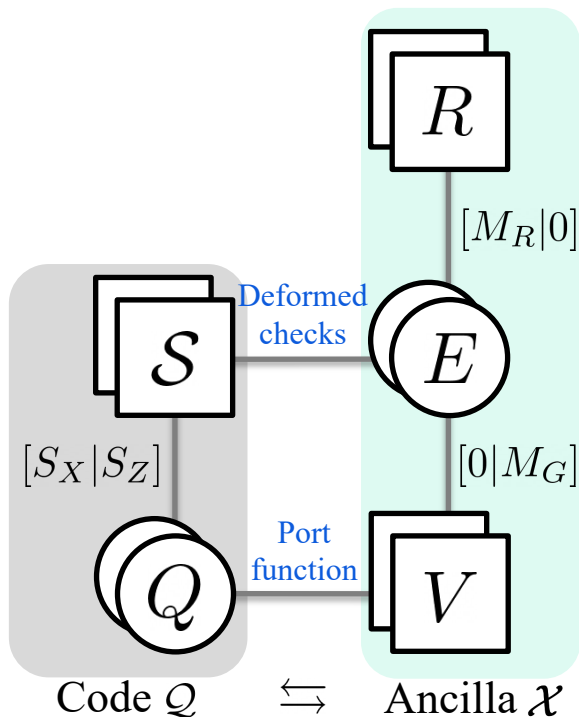
If G is a **connected simple graph**:

- Only 1 set: all the vertices. Implements one measurement.

If G is a **hypergraph**:

- Multiple sets, implements parallel measurements.

# Fault Tolerance



In phenomenological noise, we need to protect against **measurement (time-like) error** and **data (space-like) error**.

Time-like distance:

- $d$  rounds of measurement in deformed code

Space-like distance:

- The graph is **expanding**, and
- The ancilla system introduces **no new logical qubits** (measure cycle checks = gauge-fix new logicals)

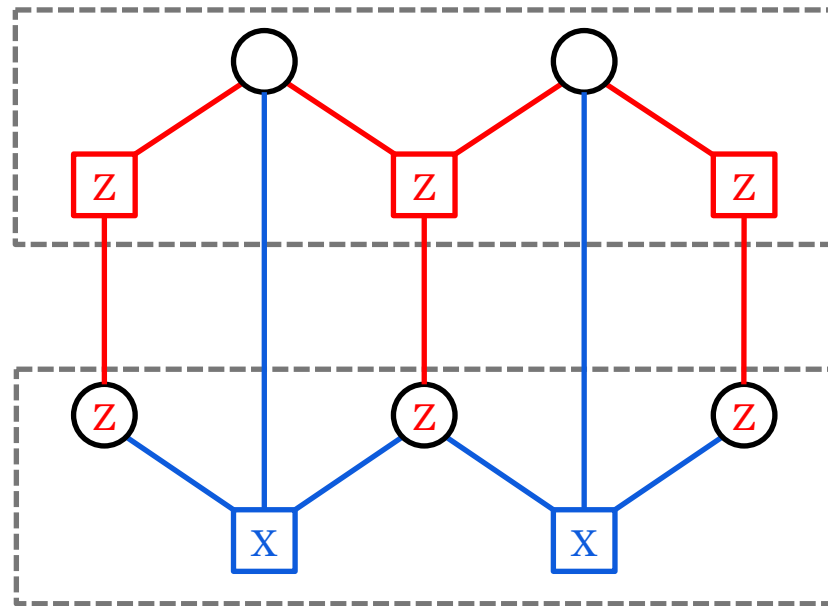
# Example

Ancilla system

Port function (1-to-1)

Check deformation:  
done with 'path matching'

Local code structure, with  
Z logical operator to be measured



○ Physical qubits    X X checks    Z Z checks

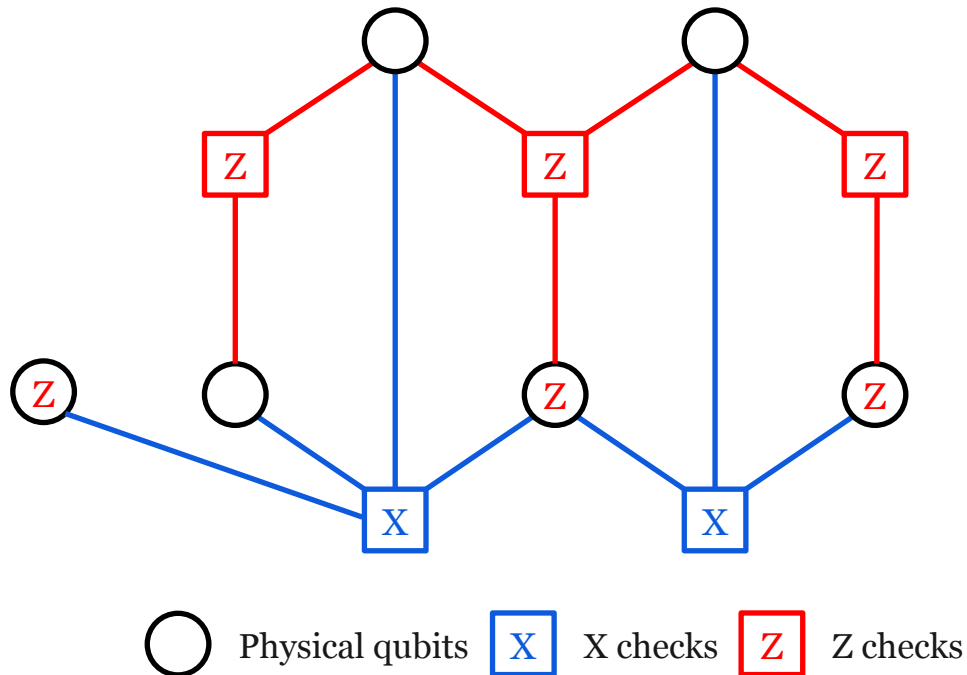
# What can go wrong?

Consider **another logical** partly supported on the physical qubits.

Its distance can be reduced in two ways:

- **Cleaning:** multiply by new stabilizers
- **Dressing:** multiply by new logicals

Let's clean with two highlighted checks



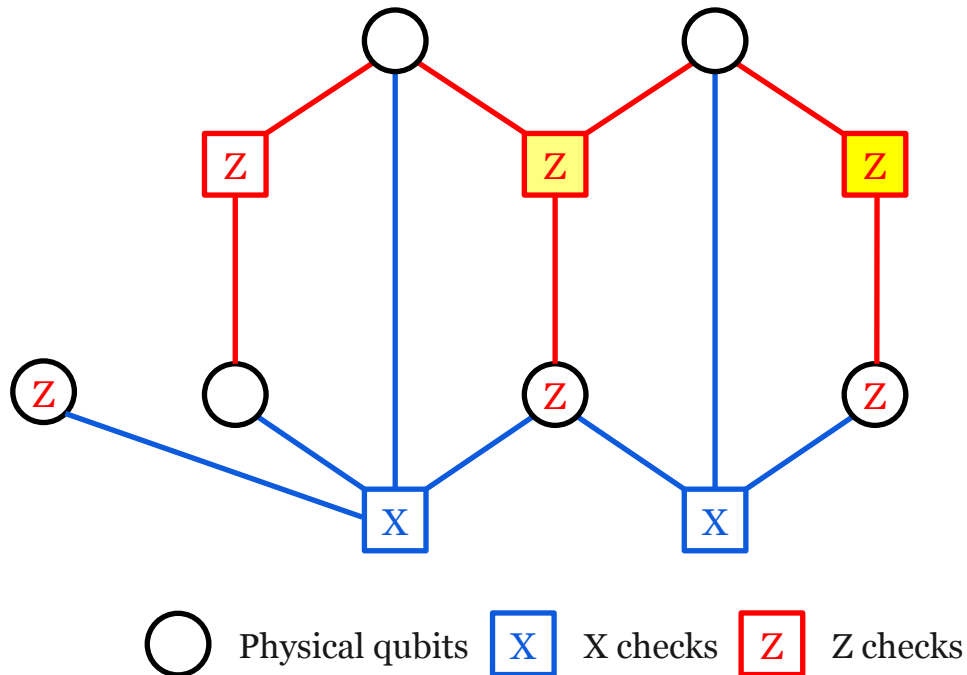
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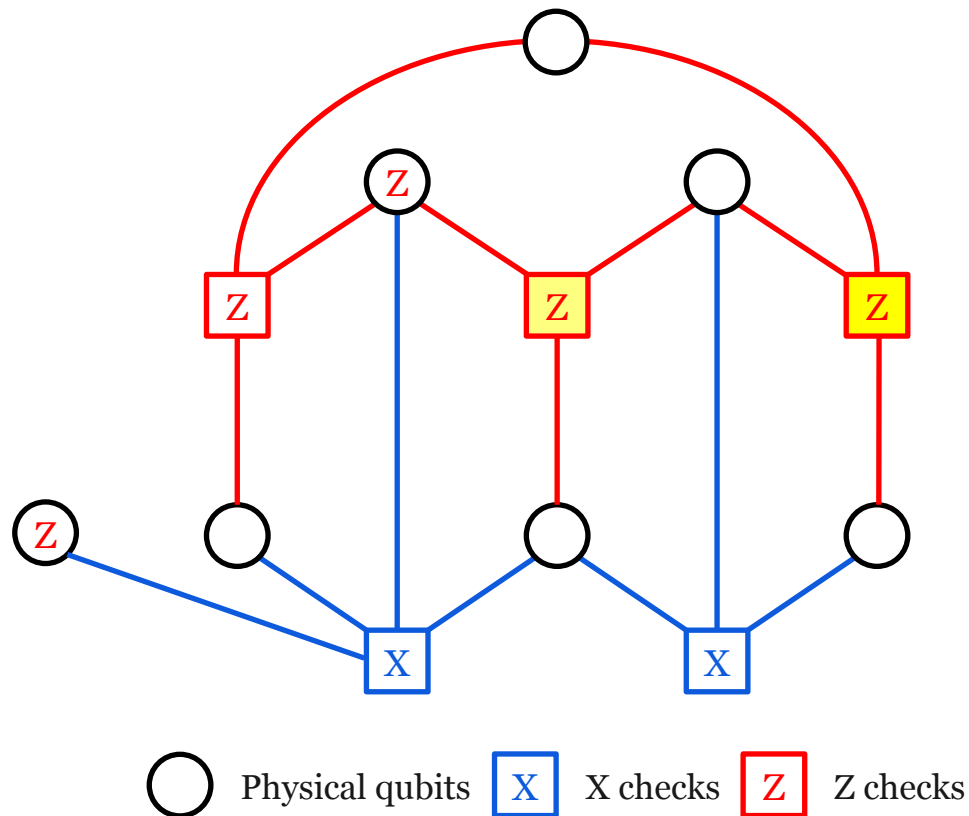
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- **Not fault-tolerant!**

Solution: **Expansion.**



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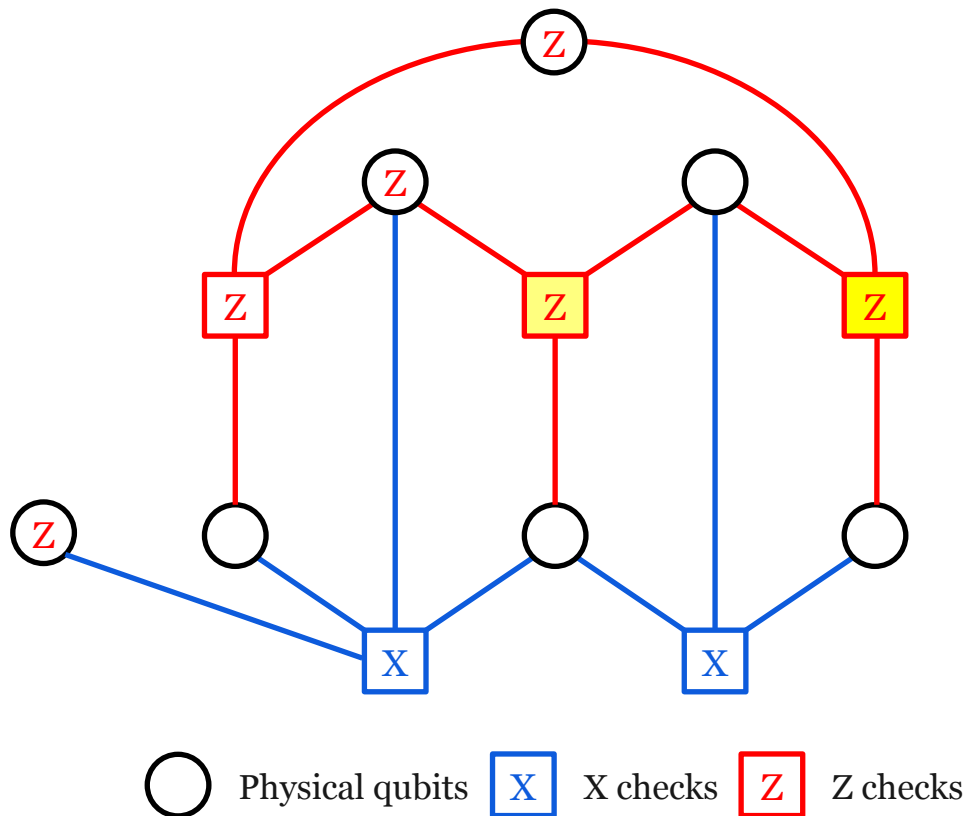
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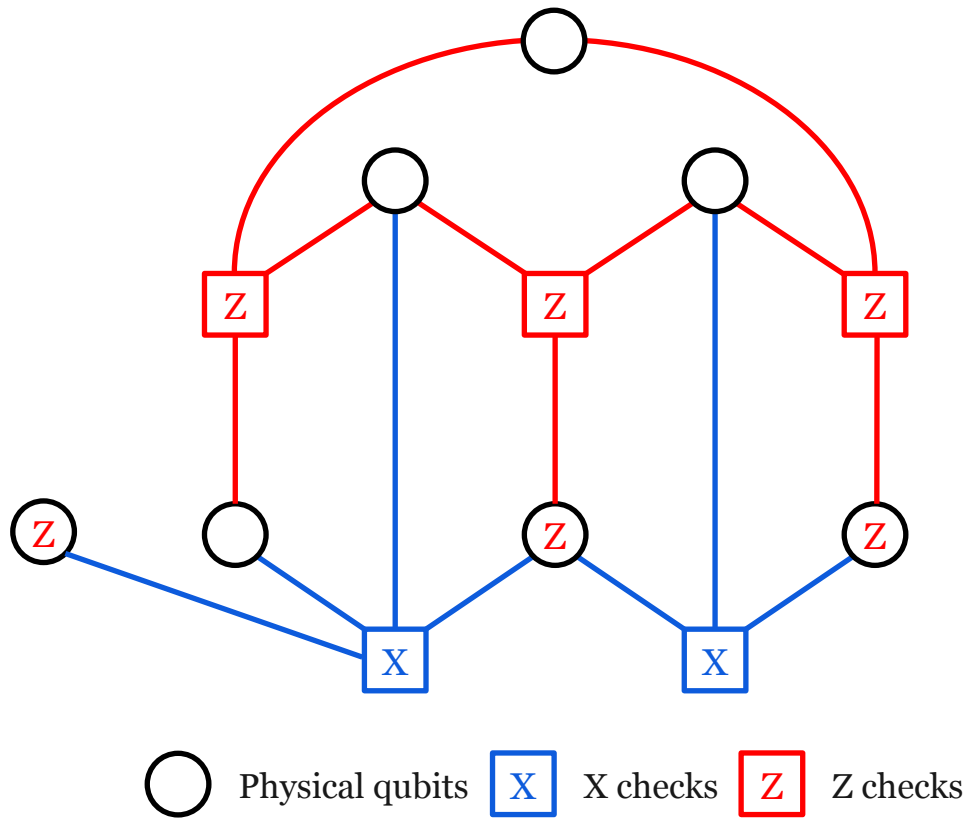
Solution: **Expansion.**

- Every two vertices now have two outgoing edges.
- Operator weight preserved by cleaning.



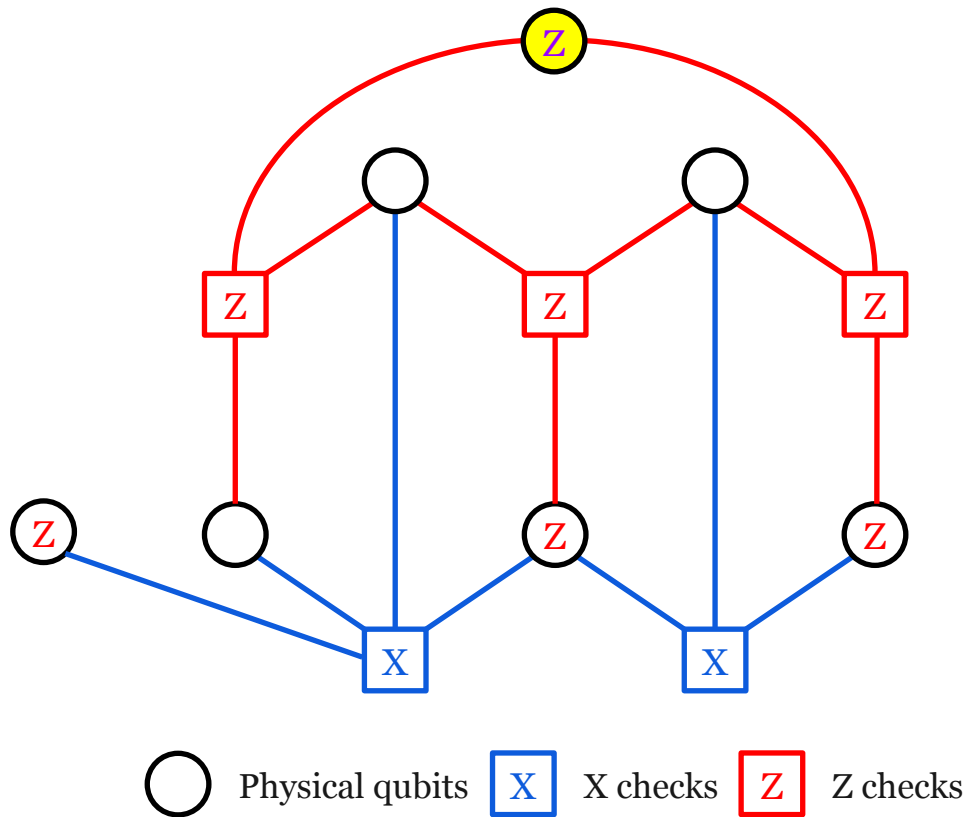
## What can go wrong (again)?

Now consider **dressing**. When we introduce more ancilla qubits than ancilla checks, we have new ‘gauge’ operators.



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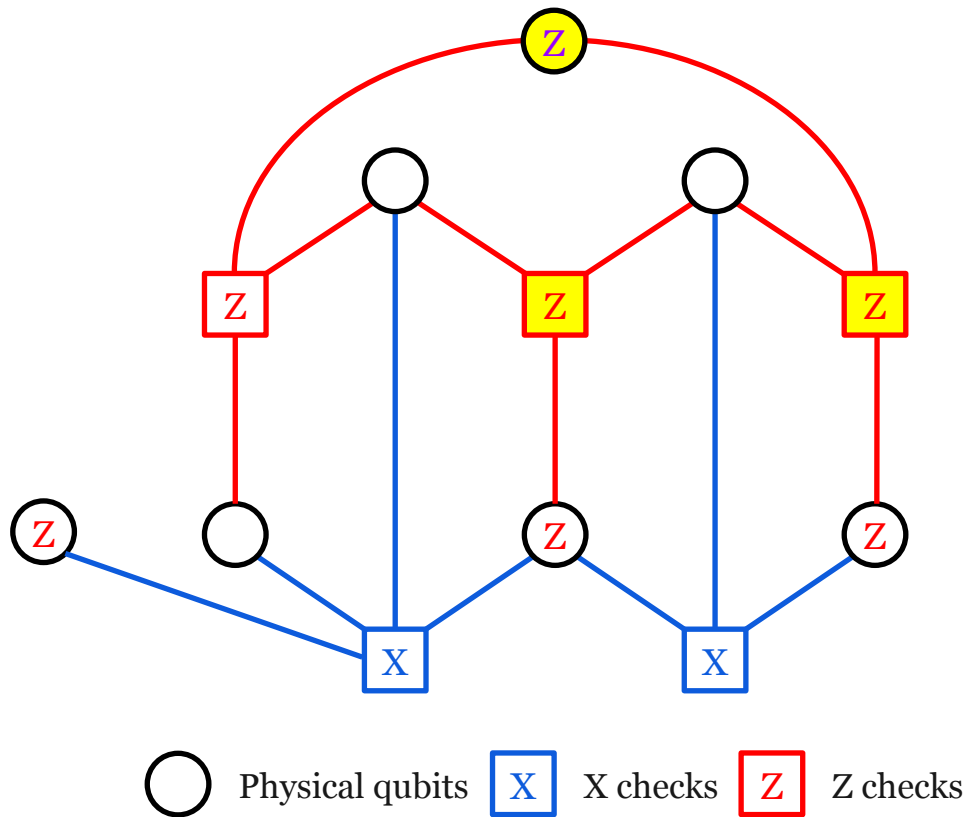
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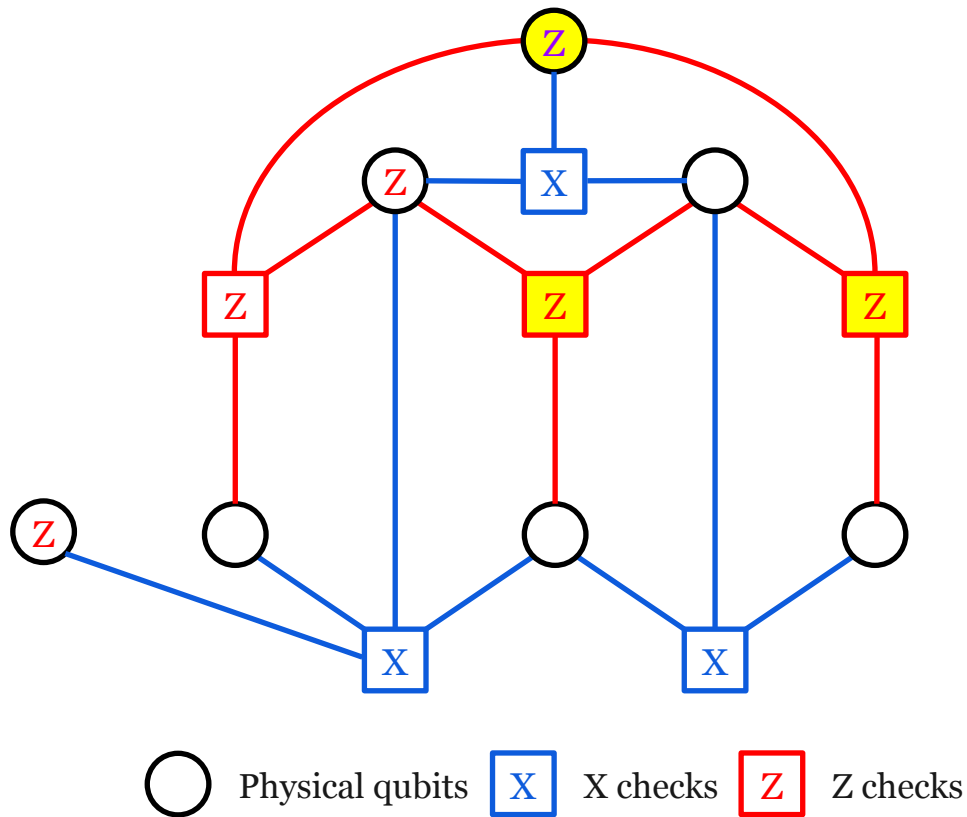
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Solution: **measure all cycle as checks in opposite basis.**

- No more new logicals  $\rightarrow$  space distance preserved.



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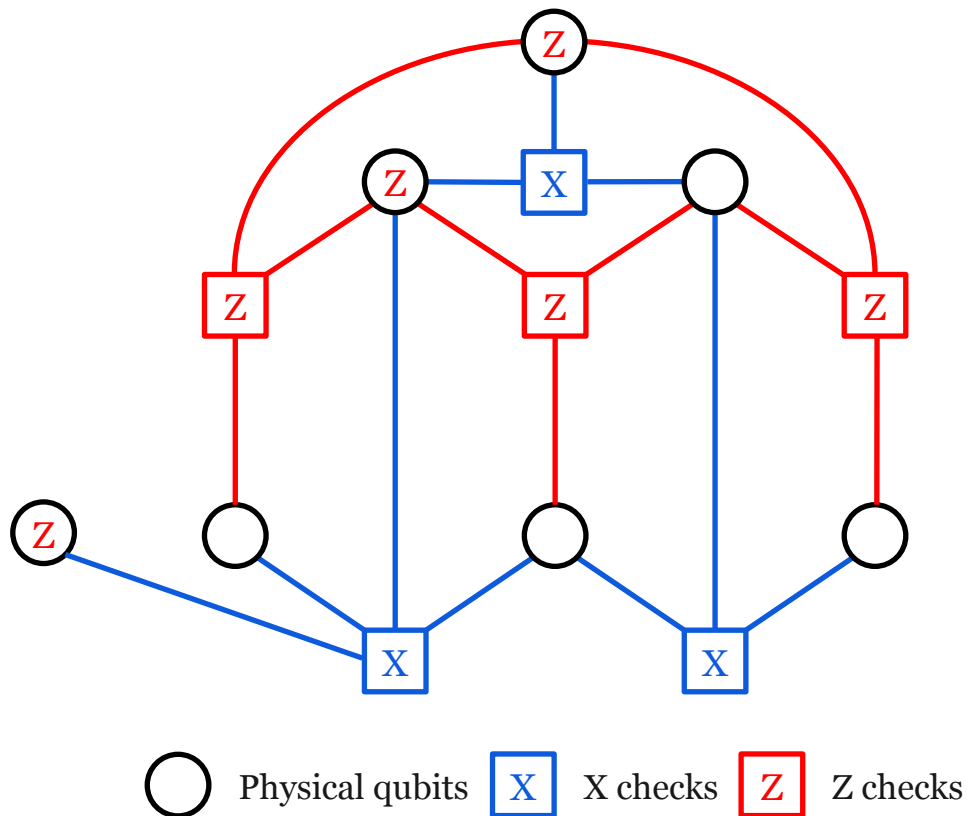
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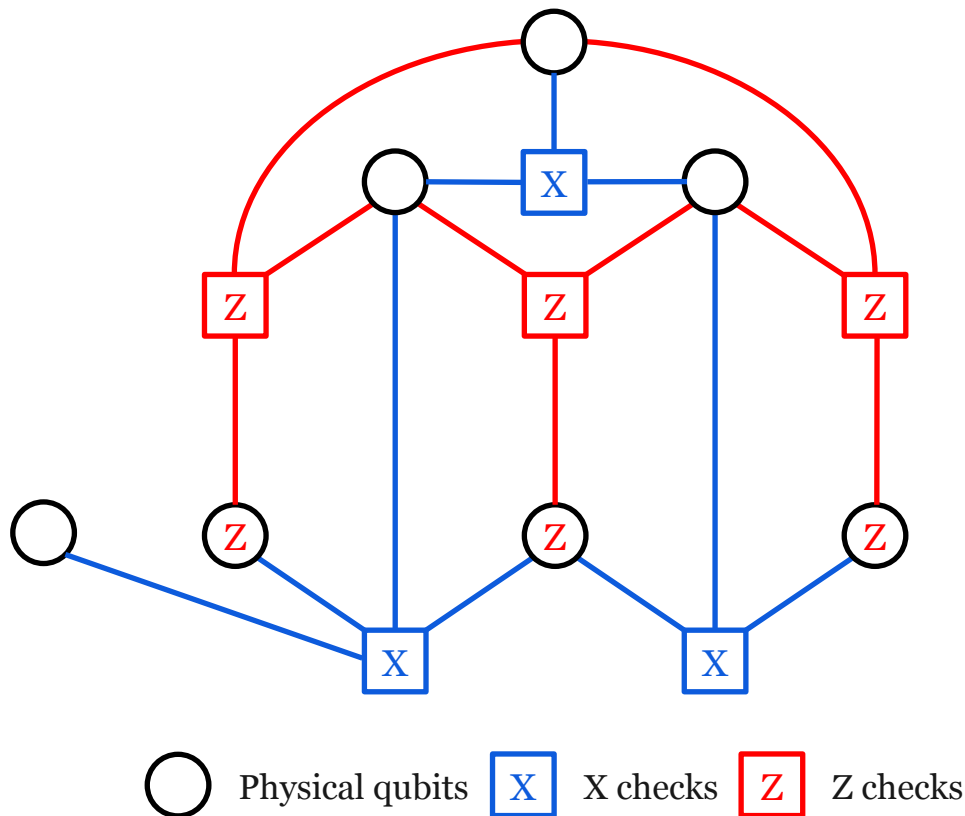
- No more new logical qubits  $\rightarrow$  space distance preserved.



# Summary: how to build graphs for surgery

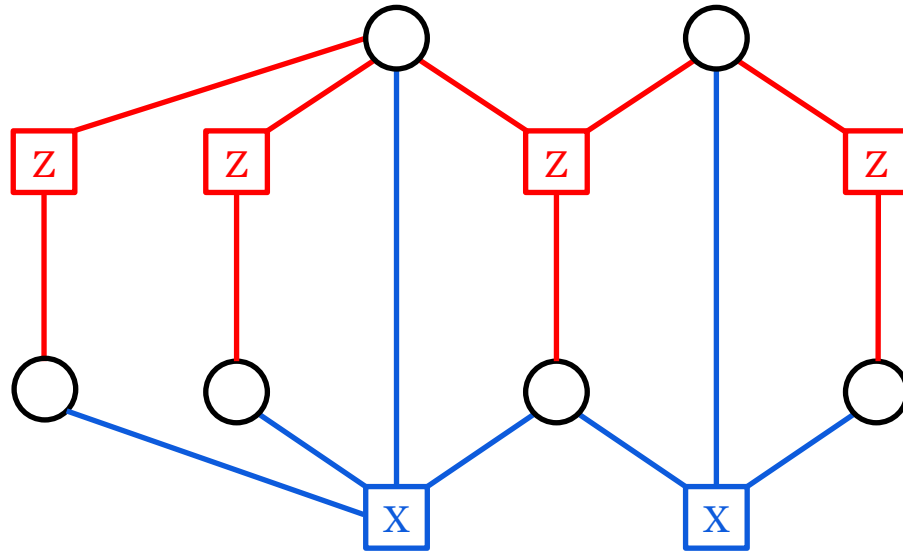
One common way to build a surgery graph for a logical operator  $L$ :

1. Create one vertex for each physical qubit
2. Port function: 1-to-1
3. Add edges ('path matchings') to ensure commutation
4. Add edges to boost expansion
5. Sparsify the cycle basis ('decongestion'), measure all cycles



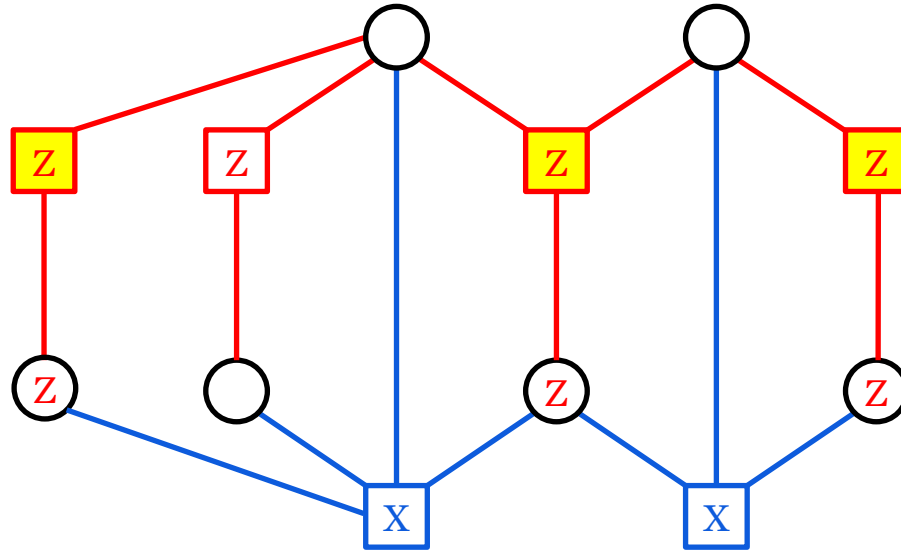
# Parallel Measurements via Hypergraphs

With a **hypergraph**, we can **measure multiple operators** at the same time.



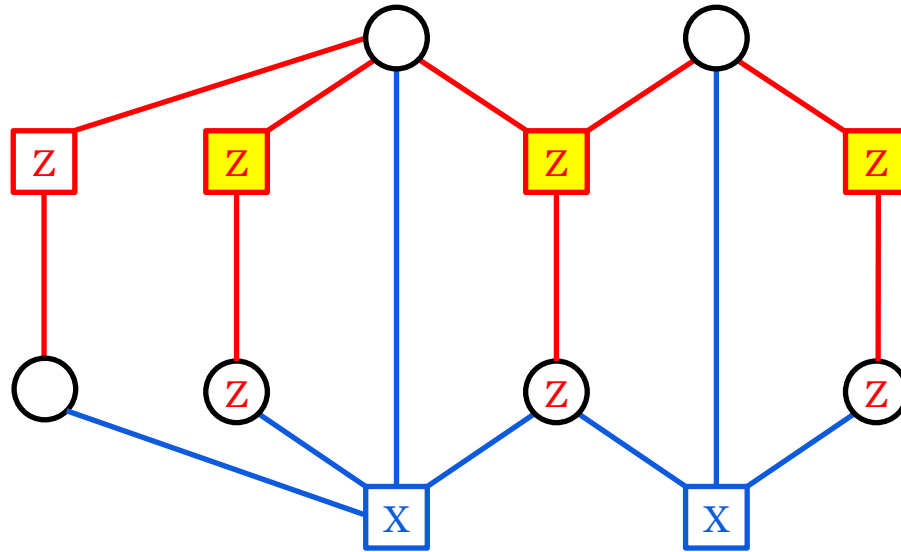
# Parallel Measurements via Hypergraphs

With a **hypergraph**, we can **measure multiple operators** at the same time.



# Parallel Measurements via Hypergraphs

With a **hypergraph**, we can **measure multiple operators** at the same time.



# **Code surgery via graphs and chain maps**

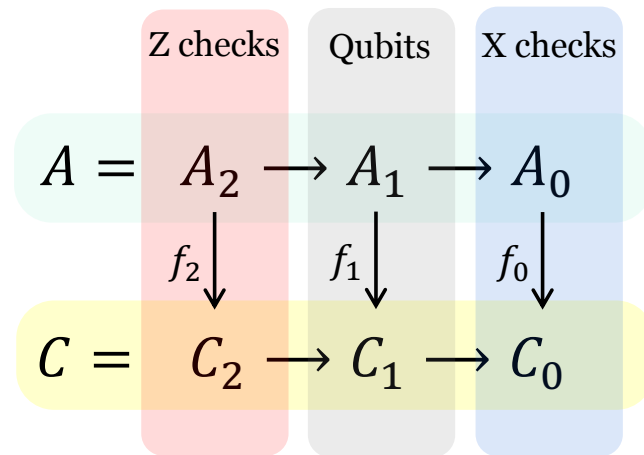
Chain map formalism

# Chain Complex and Maps

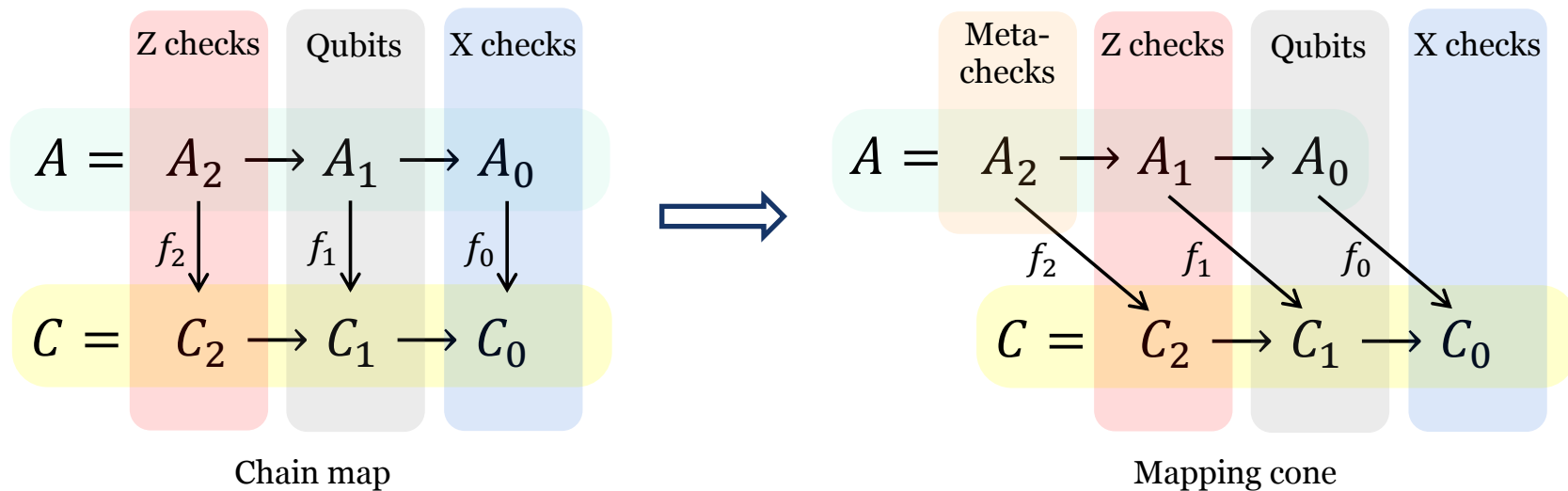
A CSS code is a chain complex. We can consider an ancilla code/complex, and maps between two complexes.

The diagram commutes  $\rightarrow$  valid chain map.

- Can be used to describe transversal CNOTs, homomorphic measurements (Steane EC).
- These maps can be trivial (o).

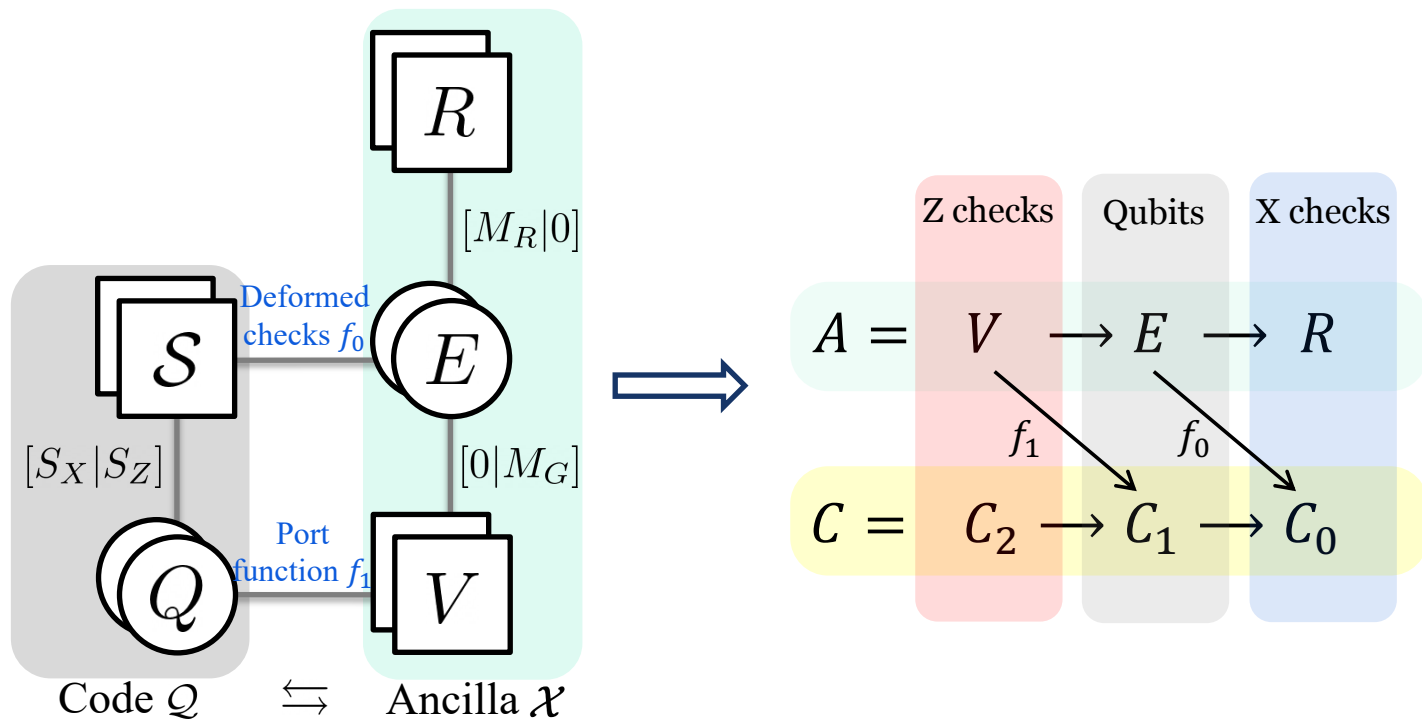


# Mapping Cone



Shift one complex by one degree. Changes operational meaning!

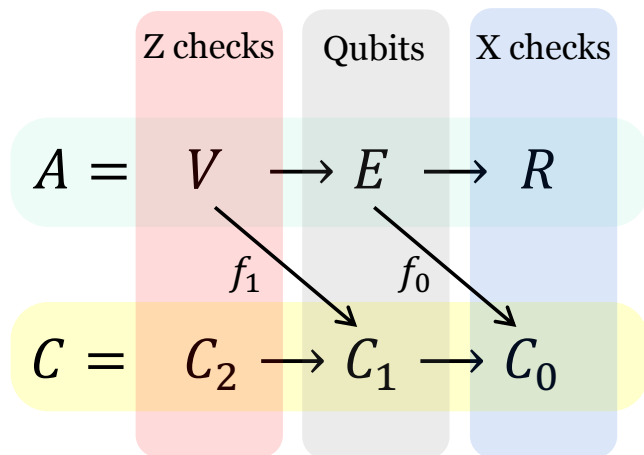
# Surgery as Mapping Cones



# Pros and Cons

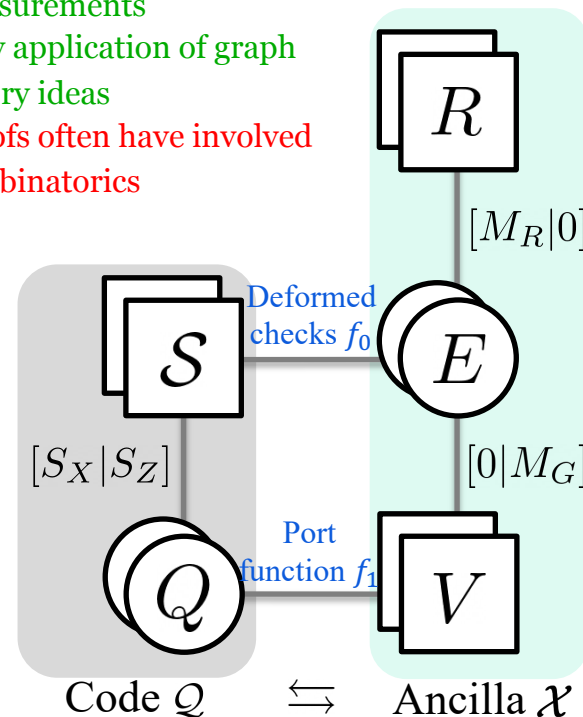
Chain map formalism:

- + More algebraic constructions and proofs
- + Easy tracking of logical qubits
- Have trouble handling non-CSS measurements and codes



Graph formalism:

- + Can easily handle non-CSS measurements
- + Easy application of graph theory ideas
- Proofs often have involved combinatorics



## **Surgery-based architectures**

# LDPC surgery via Extractors

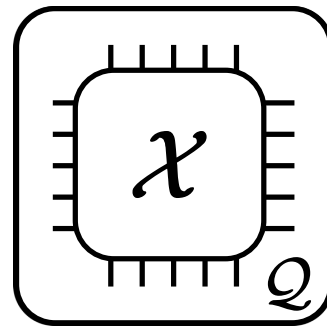
Logical control on high-rate ( $k = O(n)$ ) codes is fundamentally different from that on constant-dimension ( $k = O(1)$ ) codes. For PPMs, there are  $4^k$  many logical Pauli operators.

Current model of sequential surgery:

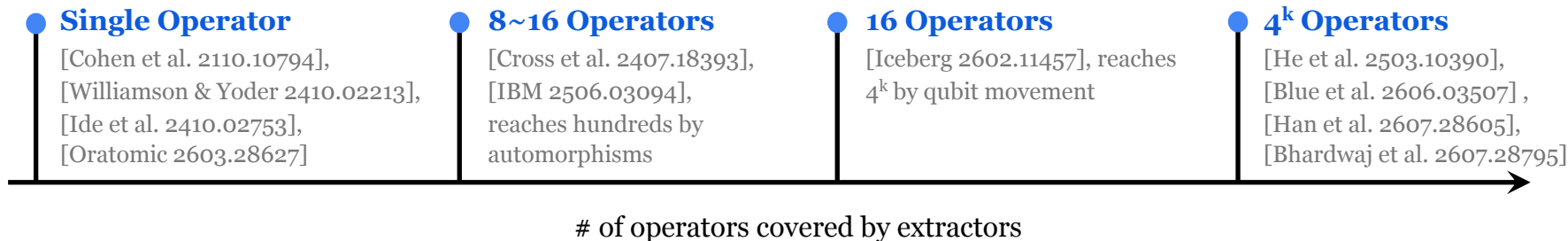
For *any* code, given *any* set of logical Paulis, can build an **extractor system** that enable measurement of *any* operator from the set, *one at a time*.

➤ Extractor size ranges between  $\tilde{O}(d) \sim \tilde{O}(n)$ .

**Key idea: extractors augment QLDPC memories into processors.**



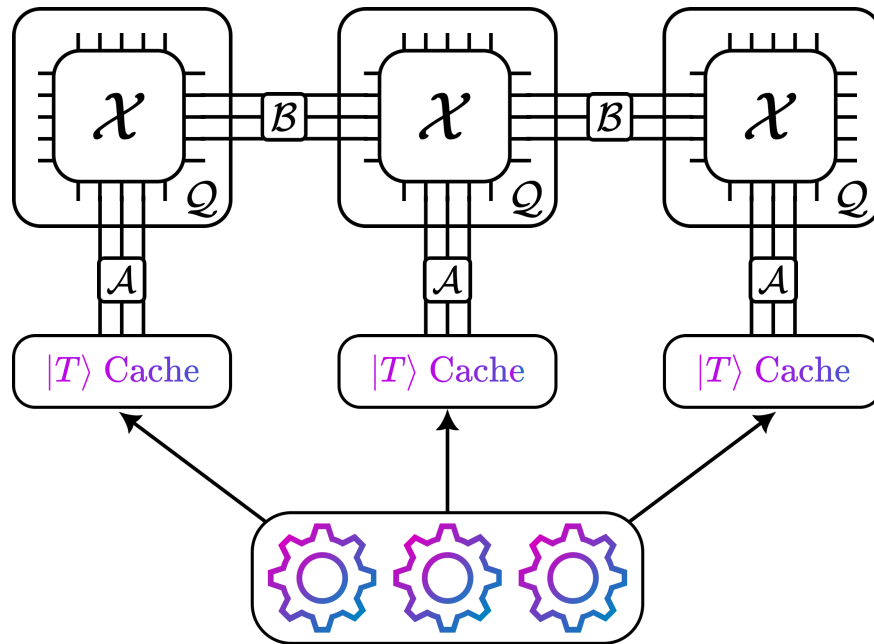
An extractor-augmented computational (EAC) block.



# Extractor architectures for Pauli-based FTQC

Building an architecture with extractors is like putting together Lego pieces:

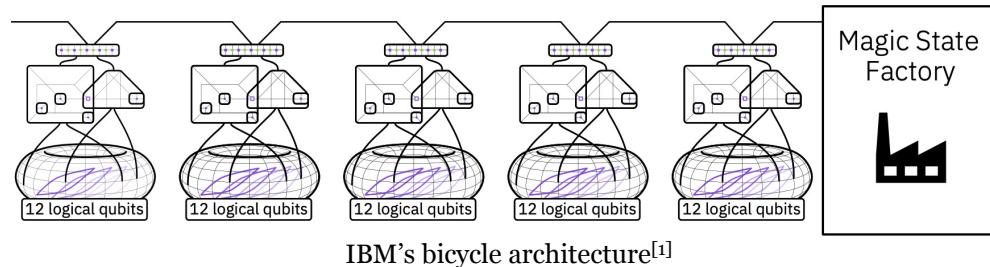
1. Choose your QLDPC codes/memory
2. Choose your logical control (PPMs) and extractor systems
  - This choice deeply impacts/depends on compilation method and resource budget!
3. Choose your magic state factories
4. Connect them up with adapters<sup>[1,2]</sup>



# Design choices of recent architectures

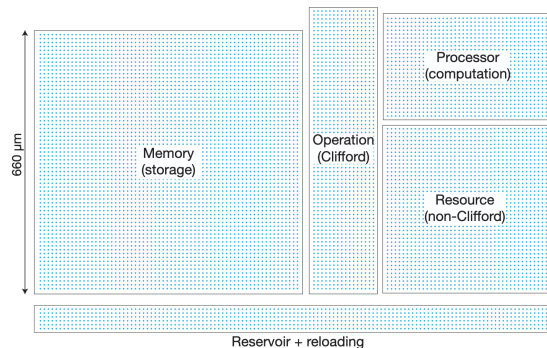
Similarity: **sequential logic**

- Every CCZ (or T) gate in the circuit is compiled into one (large) PPM. Many (or all) Clifford gates are compiled away.
- Magic state throughput is **one/logical cycle**.



Differences:

- Choice of codes – heavily impact space overhead
- Choice of extractors, including loading – heavily impacts time overhead
- Choice of magic state factories – cost of factory limits magic throughput
- Physical assumptions on qubits
- Compilation and resource estimation target
- Many more details



Oratomic's architecture<sup>[3]</sup>



- MEMORY (75 kq)
- PROCESSING UNIT (15 kq)
- MAGIC ENGINE (5 kq)

Iceberg's architecture<sup>[2]</sup>

# Demystifying the numbers

## Back-of-envelop space estimates for leading factors

**Memory:** Use high-rate codes<sup>[1-3]</sup>, ~1500 logical qubits in 5000~9000 physical qubits.

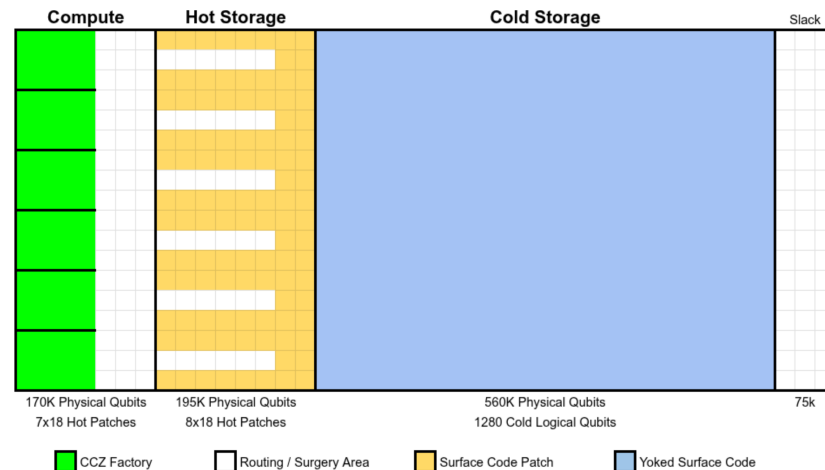
**Compute:** Can use smaller processor codes, or compute directly on memory.

- For simplicity, we can use single-operator extractors to execute large PPMs directly on memory.
- Rule of thumb: roughly the same size as memory.

**Magic states:** cultivate to d~15 surface codes, load into n~500 QLDPC codes using extractors, distill.

- Many designs ranging from 5000~35000 qubits.
- Need detailed simulation to pin down exact costs.

**Total:** 15k ~ 55k physical qubits.



Baseline: [Gidney 2025 estimate \[2505.15917\]](#)

- Surface code architecture with lattice surgery
- RSA-2048 in less than 1 million qubits, less than 1 week, on superconducting qubits
- One CCZ state per logical cycle, some parallelism in Clifford operations.

<sup>1</sup>[Kasai, 2601.08824], <sup>2</sup>[Chen et al. 2604.16209], <sup>3</sup>[Oratomic 2603.28627].

# Demystifying the numbers

## Back-of-envelop time estimates for leading factors

**Hardware:** neutral atom code cycle 1 *ms* vs.  
superconducting code cycle 1  $\mu s$ . Factor of 1000!

- Takes Gidney's 5 days to 5000 days.

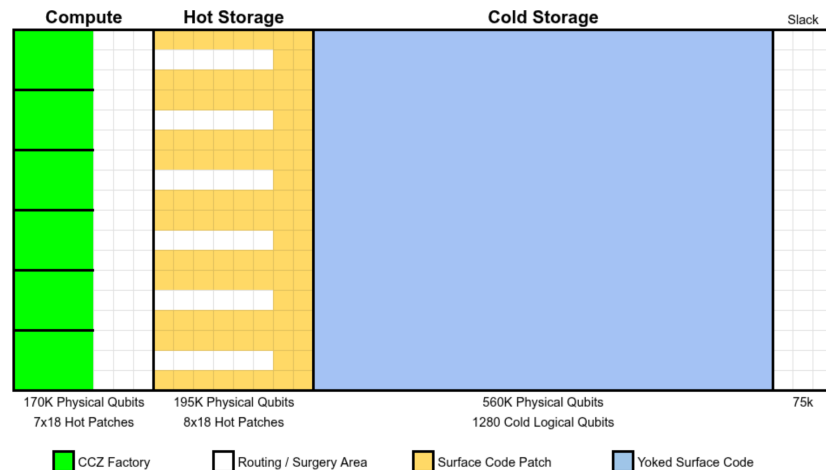
## Compilation:

- Load in/out between memory and compute;
- Compilation of PPMs;
- Choice of magic states (T vs. CCZ);
- Many more factors which depends on architectural and algorithmic choices.

## Logical clock speed:

- In current estimates, 1 logical cycle =  $O(d) \sim 20$  physical cycles. Varies with assumptions.

**Total:** on the order of 10k days.



Baseline: [Gidney 2025 estimate \[2505.15917\]](#)

- Surface code architecture with lattice surgery
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# Time overhead is not fundamental (yet)

## Magic state throughput:

- Can we do more than 1 CCZ per logical cycle?
- Can we consume more than 1 CCZ per logical cycle?



**Magic state production is the key bottleneck right now!**

- Can we design more efficient factories?
- Parallel extractors can be built for consumption.<sup>[1-3]</sup>

## Hardware: can reconfigurable qubits move faster?



Need to ask our experimental overlords. However, we can implement surgery on superconducting qubits, which are a lot faster!

## Logical cycle time:

- In current estimates, 1 logical cycle =  $O(d) \sim 20$  physical cycles
- Can this be reduced to  $O(1)$ ?



Yes! There are ways to **implement surgery with constant time overhead**.<sup>[4]</sup>

## Compilation:

- If the extractor is limited, a large PPM would need to be compiled into supported 'native instructions'
- **Leads to the 10x slow down in bicycle architecture**



Can be avoided by building a bigger extractor.

# Challenges

Building a LDPC quantum computer will not be easy! **Many challenges remain, and we need lots of solid work to resolve them.**

## Decoding:

- LDPC decoding is *much harder* than surface code decoding.
- Amazing progress in recent years, but we still need lots of work to improve speed *and* accuracy.
- **Good vs. bad decoding can lead to order-of-magnitudes difference in logical performance.**

## Hardware complexity:

- Implementing QLDPC codes & surgery won't be easy, even for reconfigurable qubits.
- **For superconducting qubits, extractors can enable universal FTQC.** However, the connectivity needed for ultra-high-rate codes (rate  $1/2$  or  $1/3$ ) is more than current assumptions.

## More QEC theory:

- To enable large-scale FTQC, we need further reduction in space-time overheads.
- Many concrete problems here.

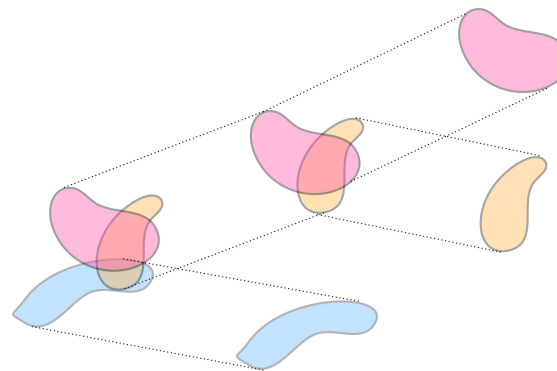
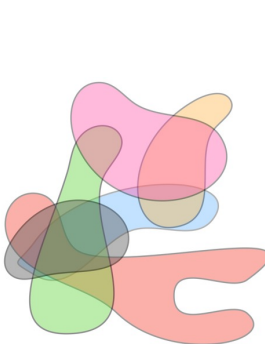
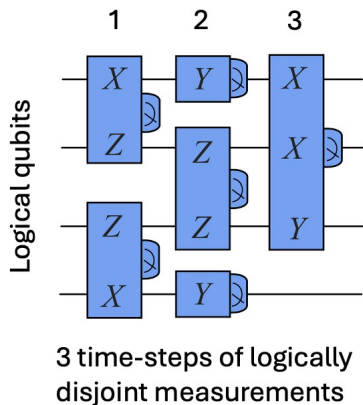
## **Further techniques in surgery**

# Parallel Surgery

Goal: measure a collection of commuting logical Pauli operators **simultaneously**.

Existing techniques:

- Use “branching” to create new copies of target logicals on an ancilla system, measure them with graph surgery.<sup>[1,2]</sup>
- Start with a surgery gadget that measures all single-logical X, puncture and/or augment it.<sup>[3]</sup>
- Heuristic construction of hypergraph surgery.<sup>[4]</sup>
- Special designs tailored to product codes.<sup>[3-7]</sup>



<sup>1</sup>[Zhang & Li 2408.01339], <sup>2</sup>[Cowtan et al. 2503.05003], <sup>3</sup>[Han et al. 2607.28605], <sup>4</sup>[Zheng et al. 2510.08523].

<sup>5</sup>[Gu et al. 2603.05398], <sup>6</sup>[Chang et al. 2603.02157], <sup>7</sup>[Bhardwaj et al. 2607.28795].

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**Caution: what operators are you measuring? How complicated are they?**

- **Parallelism alone is easy to achieve:** use transversal CNOT. What’s hard is parallel *and* addressable.
- Measuring complicated group of (non-CSS) Pauli products<sup>[1,2]</sup> costs more space than measuring many constant-logical-weight products in the same basis.<sup>[3,4,5,7]</sup>
- Both are interesting primitives, make sure to distinguish them when reading/writing a parallel surgery paper.

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<sup>1</sup>[Zhang & Li 2408.01339], <sup>2</sup>[Cowtan et al. 2503.05003], <sup>3</sup>[Han et al. 2607.28605], <sup>4</sup>[Zheng et al. 2510.08523].

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# Fast (and Parallel) Surgery

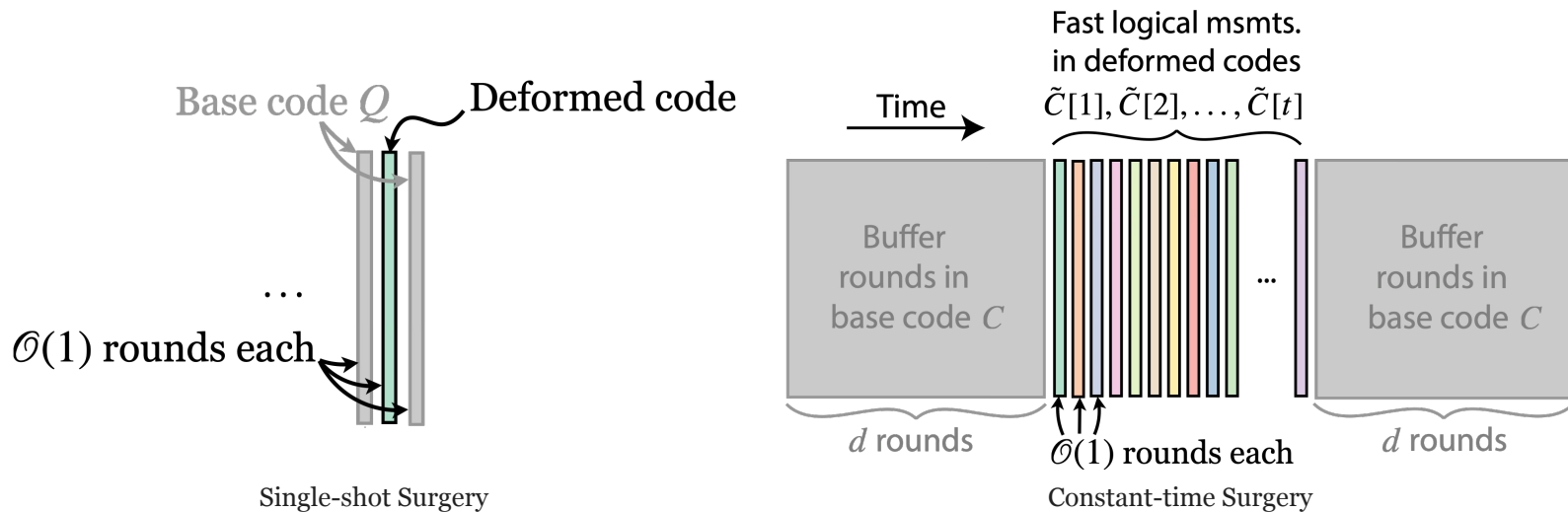
Two formulations: single-shot surgery and constant-time surgery.

**Single-shot surgery** [1-3]:

- Requires code to admit **single-shot state preparation**, such as 3D HGP codes.

**Constant-time surgery** [4,5]:

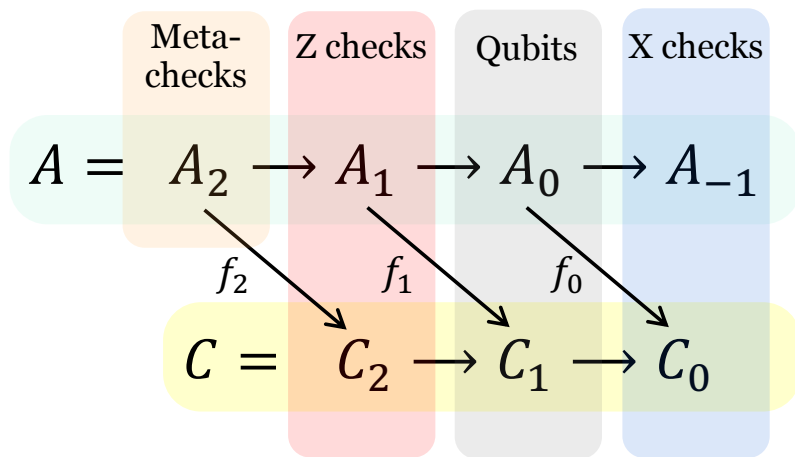
- Does not require single-shot state preparation. Akin to algorithmic fault tolerance.



# Fast (and Parallel) Surgery

Both single-shot surgery and constant-time surgery requires **meta-checks**.

- Meta-checks protect against measurement errors in vertex checks
- 4-term complex is a hypergraph → **naturally gives parallel measurements**.



# Chronicles of QLDPC Surgery

## Early weight reduction/surgery

- [H 2102.10030]
- [CKBB 2110.10794]

## Modern graph surgery formulation:

- [CHRY 2407.18393]
- [WY 2410.02213]
- [IGND 2410.02753]
- [SJY 2410.03628]

## Parallel surgery via hypergraphs:

- [ZL 2408.01339]
- [CHWY 2503.05003]
- [ZJX 2510.08523]

## Extractor Architectures:

- [HCWY 2503.10390]
- [IBM 2506.03094]
- [Iceberg 2602.11457]
- [Oratomic 2603.28627]

## Fast Surgery (single-shot)

- [HDTV 2410.12963]
- [THLGH 2510.08552]
- [BBC 2510.04521]

## Fast Surgery (constant-time)

- [CHWY 2510.14895]
- [CHYZJ 2603.02157]

## New weight reduction:

- [HLL 2510.09601]
- [YCHLW 2603.05082]

## Code-tailored Surgery/Extractors:

- [GLQXER 2603.05398]
- [BHZC 2606.03507]
- [ZZJX 2607.28605]
- [BM+ 2607.28795]

## Clifford measurements:

- [DBMWWB 2503.15751]
- [CLKS 2602.12228]
- More work upcoming.

## Applications:

- [ZZYL 2505.06981]
- [YZL 2506.18061]
- [ZZL 2510.19442]
- [XLRHD 2602.20546]

More works which we didn't include here. The field is growing rapidly.

## **Future directions**

# Future problems for QLDPC surgery

## Decoding:

- Surgery decoding has not been deeply studied. Opportunity for impactful work!
- More simulations, such as with magic state loading.

## Design of extractors:

- Can we design **constant-space-overhead full extractors** on some family of codes?  
(The space-overhead is  $\log(n)$  right now)
- Can we co-design code and extractors?

## Clifford measurements:

- Clifford measurement with surgery is a very new topic – lots to understand!

## Hypergraph sparsification:

- Can we sparsify a hypergraph (cycle basis and degree)?

Overall, lots to be discovered!

# Future directions for QLDPC architectures

## Design more efficient magic state factories

- Can we find practical codes with low-depth CCZ (or other non-Clifford) gates?<sup>[1,2]</sup>

## Structured logical control co-designed with algorithm

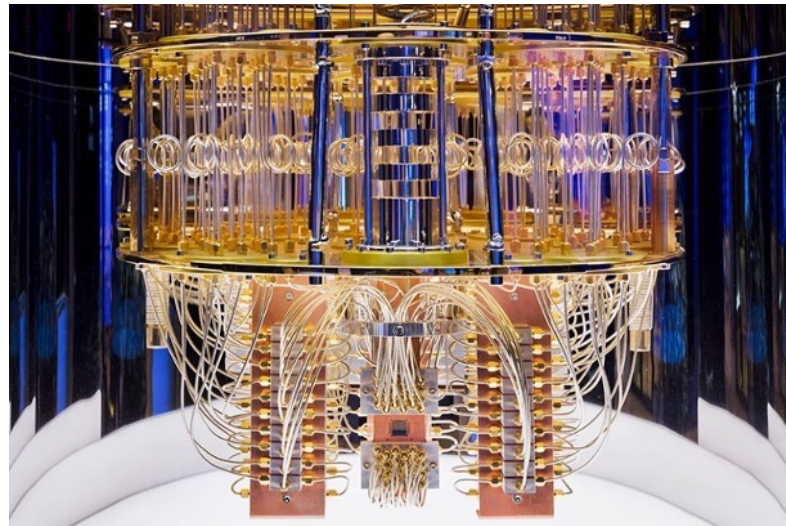
- Algorithms and their subroutines often structured. Can we design the logical control (surgery or otherwise) with respect to their structure?<sup>[3]</sup>

## Practical design of (parallel/fast/full) extractors

- Surgery is very versatile, lots of opportunity for practical/finite-scale studies.

## Is time-overhead fundamental?

- Does more efficient encoding of logical information necessarily lead to slowdown in logical computation (due to addressability or routing costs)?<sup>[4]</sup>



# Pauli-Based Computation on QLDPC Codes

A tutorial on surgery and surgery-based architectures

Sunny Zhiyang He @ Benasque, August 2026



Slides

